ARGUS Hardware Post-Processor Ideas

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Introduction

This document briefly describes a hardware implementation of an ARGUS post-processor. The post-processing in this case is a FFT and/or beamformer (not necessarily in that order.) The LVDS bus architecture of the ARGUS system enables flexible expansion due to easy duplication of LVDS data streams.

The ARGUS system currently has two possible outputs - a high data rate raw data stream (20 MSPS) from a single channel, or a low data rate channel with multiplexed channels (8-channels @ 100 kSPS.) This document is broken into two sections - each presenting a possible FFT processor implementation for high and low data rates.

1 Single Channel FFT Processor

FFT processing in software is difficult to achieve in real-time due to the high data rates. Such processing is however easily achieved in hardware. An FFT core is available from Altera [1] which can be customized. It is possible to process 14 MSPS when a 1024-point FFT is implemented using a 100MHz clock. Simulations indicate that the clock rate could be as high as 130MHz which increases the throughput to 18 MSPS.) For ARGUS, this represents almost 70-90% of the input data rate (compared to software which is only a few percent.) A possible single channel FFT processor architecture is shown in Figure 1. Here the LVDS data stream is firstly converted to a parallel form (a deserializer.) Several post-processing options exist. A Bartlett window has a simple

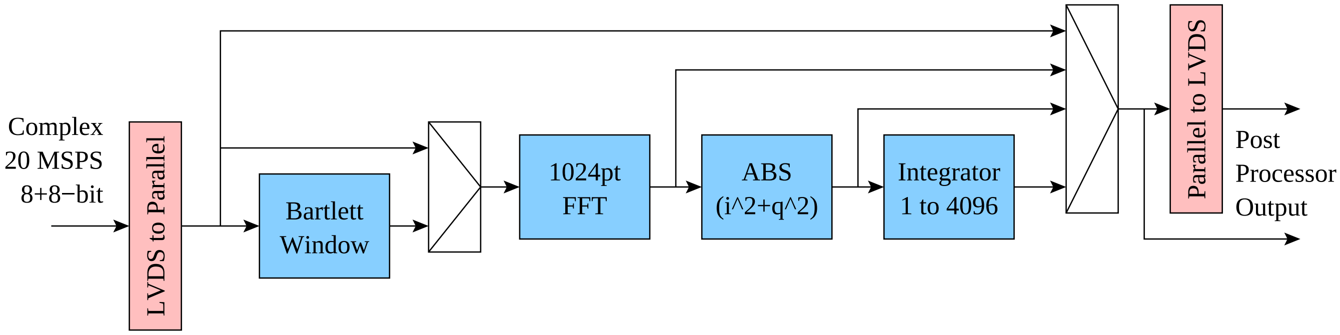


Figure 1: Example implementation of a FFT processor for an ARGUS single channel data stream (20 MSPS.) Several optional processing blocks are possible.

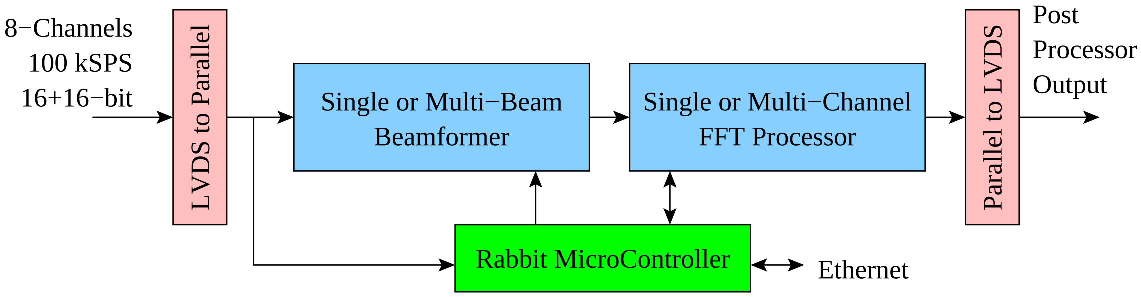
hardware implementation (a counter.) The FFT core processes 8-bit complex input data with up to 10-bit twiddle factors (10-bits is optimal for a 1024-point FFT.) The FFT output can then be be spectrally integrated up to a desired number of integrations. Each blocks output data can be selected for the post-processor output. The output data can be in a parallel form (to a PCI-DIO-32HS digital I/O card) or alternatively back to LVDS. The LVDS output could then be further post-processed, for example, in a correlator.

This type of post-processing architecture could possibly be implemented in a EP20K-160EQC208-1 Altera FPGAs ($250 each) depending on the desired functionality. This would bring the total cost for a module to be around $400.

2 Multi-Channel Post-Processor

A multi-channel post processor has many more processing possibilities due to the greater number of simultaneous channels. Processing could include FFT, beamforming, correlation, etc.. The number of channels is traded off for bandwidth. In the current ARGUS system we have 8 channels, each with 100kHz of bandwidth. Due to the low bandwidth of each channel it is possible to perform 1024pt FFTs in real-time. Larger FFTs can be performed but memory is at a premium.

Figure 2 illustrates an example beamformer post-processing option. Beamforming is an operation than can easily be performed (since the input data is already channel multiplexed) with a single complex multiplier (single beam operation) and a register file containing beamformer weights. Given sufficient FPGA space multiple beams could be formed simultaneously. Alternatively, the multiplier could be clocked at higher frequencies (e.g. 64 × 100kHz= 6.4MHz) to form more beams. Depending on the number of beams formed a single or multi-channel FFT processor can post-process the beams.



(a) Beamformer followed by FFT

Figure 2: Example implementation of a multi-channel beamformer followed by a FFT processor.

A single channel FFT processor is easily implemented due to the very low data rates (100kSPS for example.) Such an FFT processor would only require a 1MHz clock to perform the transform in real-time. Alternatively, 64 transforms (of beams or data) could be performed with a 64MHz clock.

A Rabbit micro-controller could be used to control the system - set the beamformer weights, control the FFT post processing, etc.. Additionally, given that there is significant integration performed in hardware - the output data rate might be slow enough that the Rabbit could read the results and transmit the data across the local network.

Figure 3 illustrates an example multi-channel (data or beam) FFT post-processor (for 8 channels.) External memory is required to buffer the input data. This input data has to de-multiplexed into SRAM before it can be processed channel-by-channel in the FFT processor. The amount of memory depends on the number of channels to be processed.

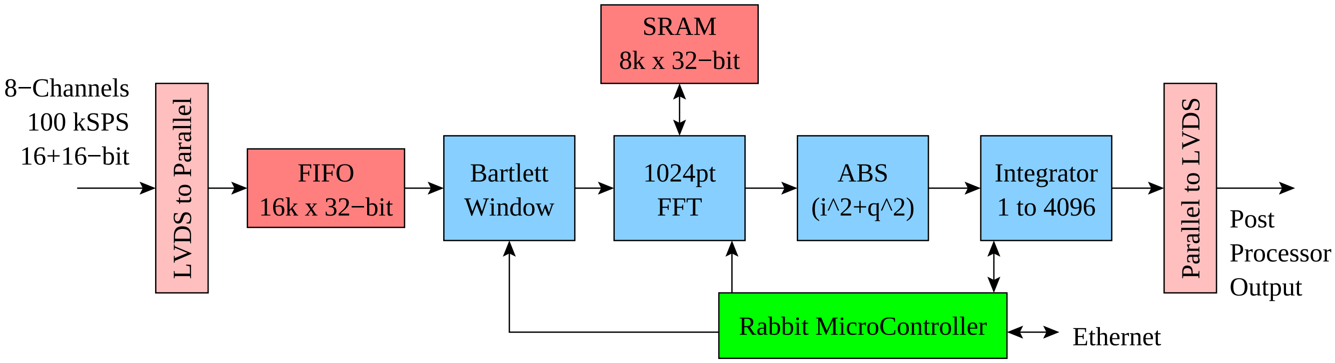


Figure 3: Example implementation of a multi-channel (beam or data) FFT and spectral integrator.

The required FPGA hardware varies considerably depending on what type (and how much) processing will be done. Due to the much lower data rates many more processing options are available. Additionally, since the FFT clock rate is much lower, then lower speed grade FPGAs can be used to perform the processing. For example, a single channel beamformer and FFT starts at around a $100. A multi-beam and multi-FFT system requires additional memory and larger FPGA, so a total cost around $300 would be expected.

Summary and Conclusions

This report has presented some post-processing implementation ideas for the ARGUS system. Many post-processing possibilities exist for ARGUS due to the flexibility of data transport using LVDS. Due to the low data rates it is possible to implement multi-channel processing with little added cost.

References

[1] *FFT MegaCore Function User Guide*, Altera Corporation, March 2001. http://www.altera.com/literature/ug/fft_ug.pdf.