The Argus "2002" Architecture

Steven W. Ellingson[1]

[1] The Ohio State University ElectroScience Laboratory, 1320 Kinnear Road, Columbus OH 43212. E-mail: ellingson.1@osu.edu

I. Acronyms

ANP Argus Narrowband Processor

DDC Digital Downconverter (here, the Analog Devices AD6620)

DCR Direct Conversion Receiver (here, an ESL-built receiver module)

DRP Digital Receiver/Processor (here, an ESL-built circuit board)

ESL ElectroScience Laboratory

kSPS Thousand samples per second

LAN Local Area Network

LVDS Low-Voltage Differential Signaling

MSPS Million samples per second

PC Personal Computer (i.e., a self-contained desktop computer)

UDP/IP User Datagram Protocol / Internet Protocol

II. Introduction

"Argus" is a concept for a radio telescope that has an instantaneous field of view covering most of the visible sky [1]. Presently, the primary motivation for this concept is to facilitate a microwave SETI program targeting strong ultra-narrowband signals incident from anywhere in the sky [2]. A prototype development project is underway at the Ohio State University ElectroScience Laboratory (ESL), with the interim goal of implementing a 64-element Argus system.

This document describes the current architecture for the ESL Argus system, referred to here as the "2002" architecture. The term 2002 refers to the year in which the architecture was conceived, and we use this term to descriminate this architecture from previous architectures with which we have experimented [3]. Elements of the 2002 architecture are already described in a detailed design report [4]. The purpose of this report is to provide a high-level overview, and to more clearly explain the capabilities and limitations of this architecture.

III. Goal ($N = 64$) Architecture

An overview of the goal 64-element architecture is shown in Figure 1.

A. DCR

A Direct Conversion Receiver (DCR) is used to convert a 14-MHz swath of spectrum within the tuning range of 1.2–1.8 GHz into a complex-valued digital signal consisting of 8-bit + 8-bit samples at 20 MSPS. This is converted into a 320 Mb/s serial data stream for transmission using Low-Voltage Differential Signaling (LVDS). The LVDS signal from each DCR is carried on off-the-shelf CAT-5 ethernet cable. The design of the DCR is documented in [4].

B. ANP

The central element of the 2002 architecture is the Argus Narrowband Processor (ANP). The ANP accepts the output from up to 64 DCRs, selects a swath of about 8 kHz from the 14 MHz passband for further processing, organizes the array output into snapshots (sets of samples consisting of one sample from each element of the array taken at the same instant), and finally broadcasts the snapshots across a 100baseT ethernet network.

A functional block diagram of the ANP is shown in Figure 2. The ANP consists of $N = 64$ digital receiver/processors (DRPs), one Array Controller, and one PC.

B.1 ANP: DRP (Card)

A DRP is a single circuit board which accepts the 320-Mb/s data stream from one DCR, reformats it as parallel data, processes it through a digital downconverter (DDC), and then re-serializes the result for output. The DRP is documented in detail in [4]. The DDC used here is the single-chip Analog Devices AD6620, which is able to downconvert any frequency within the 14 MHz passband to a frequency of zero, lowpass filter the resulting I and Q components to set a narrower bandwidth, and then decimate (reduce) the sample rate accordingly. In the $N = 64$ architecture, the planned decimation rate $R = 500$, resulting in an output sample rate of 40 kSPS and a passband about 8 kHz wide. Also, the sample size grows to 32 bits; i.e., 16-bits I + 16-bits Q. As will be discussed later, the ANP is actually capable of greater decimated sample rates internally, but 40 kSPS $\times$ 32 bits/sample $\times$ 64 elements = 81.92 Mb/s, which is close to the 100-Mb/s limit of the 100baseT output path.

B.2 ANP: Daisy Chain (Backplane)

To organize the DRP output samples into snapshots, a "daisy chain" serial bus architecture is used. This is illustrated in Figure 2. The DRPs are connected in series by LVDS links. Each DRP receives all the samples output by the DRPs before it, adds it's output sample, and passes along the set to the next DRP. Also part of the daisy chain is an array controller, described below, which manages the operation of the daisy chain. In the Goal $N = 64$ architecture, the daisy chain runs at 81.92 Mb/s. (However, the prototype system has been tested at rates up to 204.8 Mb/s and rates up to 320 Mb/s should be no problem.)

B.3 ANP: Array Controller (Card)

The array controller card collects the snapshots assembled using the daisy chain and outputs them in 16-bit parallel fashion. In the Goal $N = 64$ architecture, this happens at 5.12 MW/s.

B.4 ANP: PC

The 16-bit words output by the Array Controller Card are received via a National Instruments DIO-32HS board mounted in a PCI slot in a Windows 98 PC. Using a C-Language program, these samples are relayed to a 100baseT ethernet card (also on the PCI backplane) and broadcast across a dedicated LAN using UDP/IP at 81.92 Mb/s.

C. Computing Engine

The snapshots broadcast from the ANP using a UDP/IP LAN are received by a bank of PCs running Linux. The PCs are organized by the System Control PC (a single PC which has overall control of the Argus system) to acquire sets of contiguous snapshots and process them. Normally, the computational burden associated with processing a single ANP output will be more than one PC can handle. In this case, the System Control PC organizes the computing engine PCs such that they take turns accepting data from the UDP/IP broadcast. This concept was originally developed in [5] and is explained in some detail there. The output from each computing engine PC is minimal; limited to (nominally) infrequent alarms and periodic status/control traffic. This is handled using a

separate TCP/IP LAN; i.e., each computing engine PC is dual-homed.

D. Special Functions Accomodated by the ANP

The daisy chain architecture of the ANP makes it straightforward to implement additional processing using additional cards. Examples of in-line processing include on-the-fly calibration and RFI mitigation. Such cards could also be used to provide a path out of the system which is transparent and non-disruptive to existing system. Examples might include special, dedicated beamformers with real time outputs, and interfaces to completely different systems.

E. Bandwidth Expansion via DCR Output Replication

Note that the bandwidth processed by the ANP is nominally about 8 kHz for $N = 64$, whereas each DCR provides 14 MHz of bandwidth. However, it is straightforward to "fan out" the LVDS output as many times as necessary. Thus, up to 14 MHz of bandwidth can be processed simply by replicating DCR outputs an implementing the additional ANPs and computing engines. Of course, a very large number of ANPs are required to cover the full 14 MHz; approximately 1750 to be specific.

References

[1] R.S. Dixon, "Argus: A Next-Generation Omnidirectional Radio Telescope," *Proc. High-Sensitivity Radio Astronomy*, University of Manchester, England, January 1996. Reprinted in N. Jackson and R.J. Davies, *High-Sensitivity Radio Astronomy*, Cambridge University Press, 1997, pp. 260-8.

[2] J. Tarter, J. Dreher, S.W. Ellingson, and W.J. Welch, "Recent Progress and Activities in the Search for Extraterrestrial Intelligence (SETI)," Chapter 36 of *Review of Radio Science, 1999-2002*, W. Ross Stone (Ed.), IEEE Press/John Wiley, 2002.

[3] ESL Argus Document Server, http://esl.eng.ohio-state.edu/∼swe/argus/docserv.html.

[4] G. Hampson and S. Ellingson, "A New Argus Direct Conversion Receiver and Digital Array Receiver/Processor," Design Report, September 27, 2002. Available at http://esl.eng.ohio-state.edu/∼swe/argus/docserv.html.

[5] T. Alferink, *A Digital Signal Processing Engine for a Large Antenna Array,* Master's Thesis, The Ohio State University, 2000.

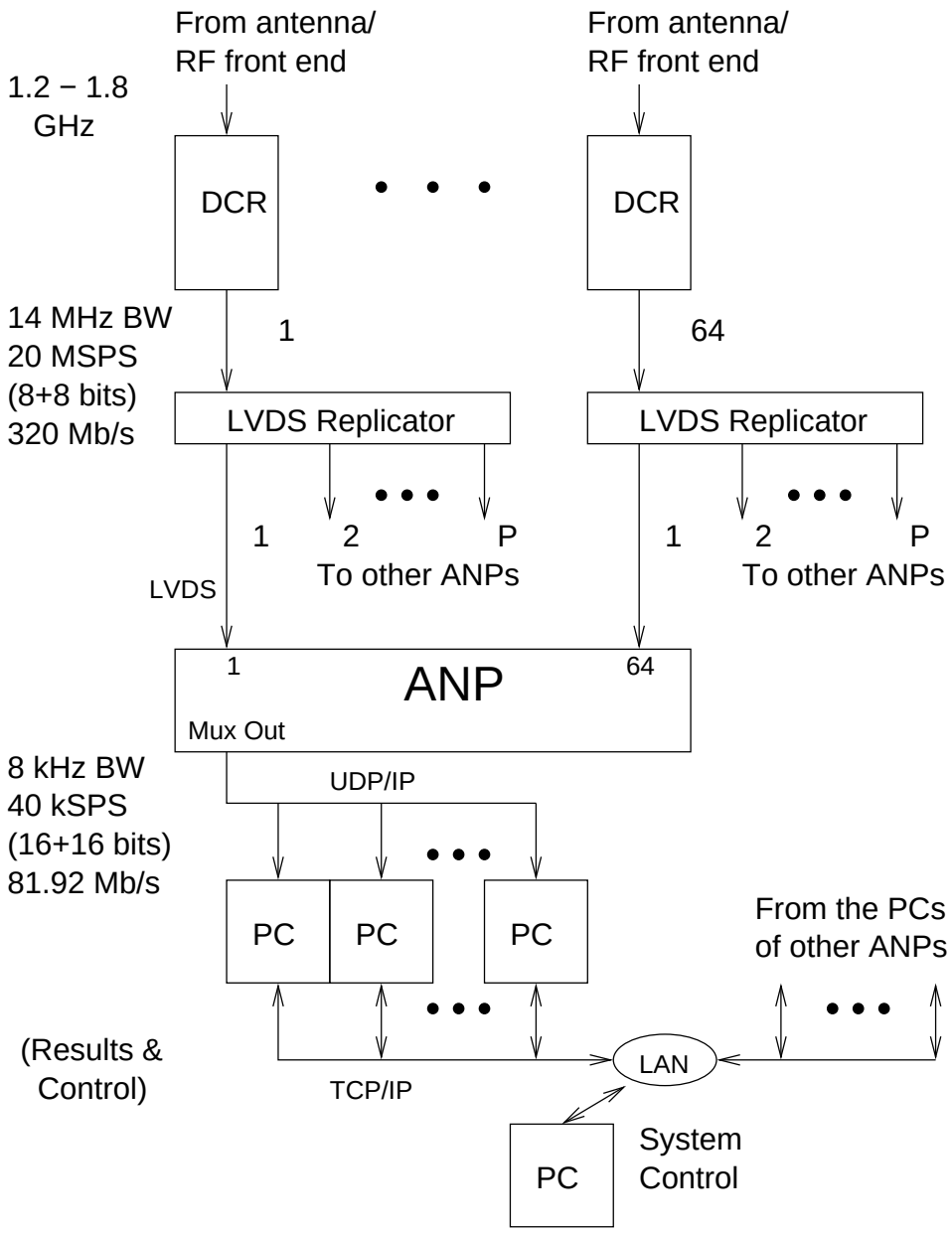

Fig. 1. Overview of the goal ($N = 64$) architecture.

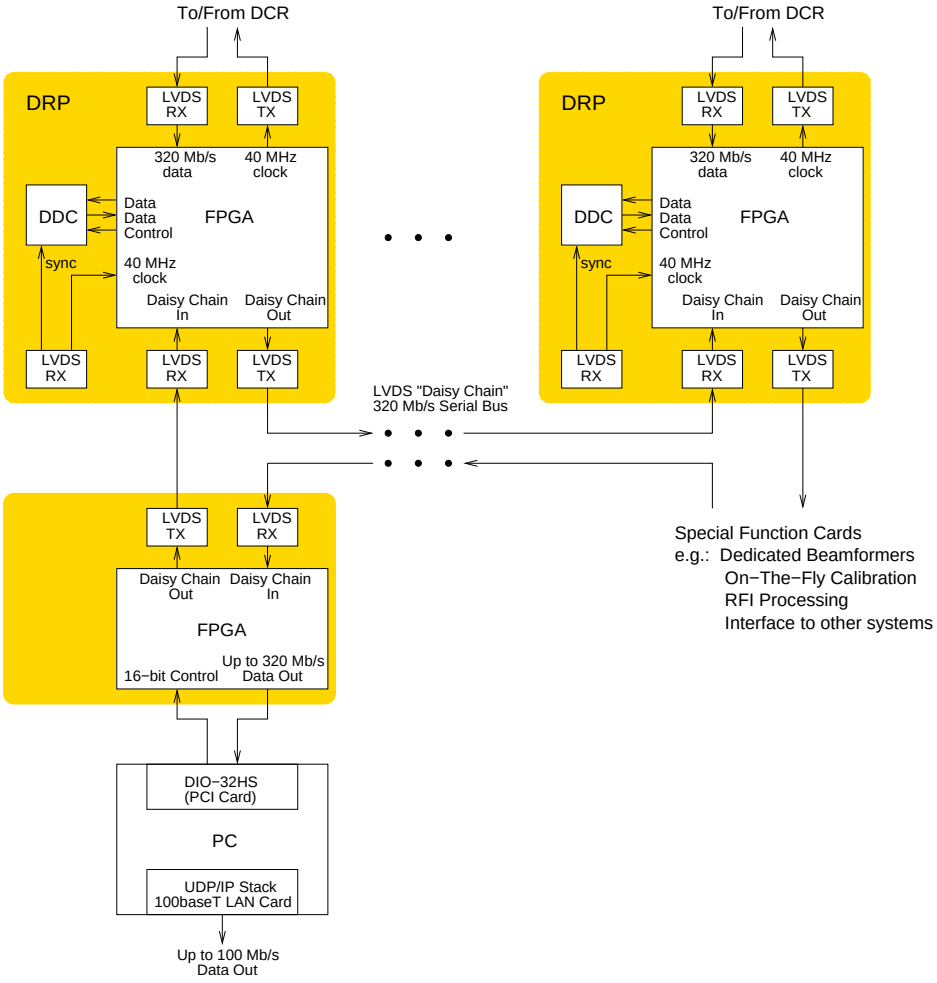
To/From DCR
To/From DCR
DRP
LVDS RX
LVDS TX
320 Mb/s data
40 MHz clock
DDC
Data
Data
Control
FPGA
sync
40 MHz clock
Daisy Chain In
Daisy Chain Out
LVDS RX
LVDS RX
LVDS TX
DRP
LVDS RX
LVDS TX
320 Mb/s data
40 MHz clock
DDC
Data
Data
Control
FPGA
sync
40 MHz clock
Daisy Chain In
Daisy Chain Out
LVDS RX
LVDS RX
LVDS TX
LVDS "Daisy Chain"
320 Mb/s Serial Bus
LVDS TX
LVDS RX
Daisy Chain Out
Daisy Chain In
FPGA
16−bit Control
Up to 320 Mb/s Data Out
Special Function Cards
e.g.: Dedicated Beamformers
On−The−Fly Calibration
RFI Processing
Interface to other systems
DIO−32HS (PCI Card)
PC
UDP/IP Stack 100baseT LAN Card
Up to 100 Mb/s Data Out

Fig. 2. ANP